REMARKS

The examiner has rejected Claims 1-3, 6-8, and 10-11 as being anticipated under 35 USC 102 (e) as being anticipated by Steeley, PGPUB US 2002/0099913 A1. The examiner has also rejected claims 4 and 5 under 35 USC 103 as being obvious over Steeley, claim 9 as being obvious over Steeley in view of Chaudhry, et. al., PGPUB US 2002/0152359 A1, and claim 12 as being obvious over Steeley in view of Syed, et al, PGPUB US 2002/0108021 A1.

Claims 1-3, 6-8, and 10-11.

Revisions to Claims 1

Claim 1 has been revised to more clearly state that the upper and lower level valid bits belong to the same tag memory.

Claim Rejections

As cited by the Examiner in section 3, line 3-5, Steeley discloses a set-associative cache (para. 7) having tag memory (para. 15) coupled to be addressed by the tag index portion of the cache line address. Further, the tag memory of Steeley has at least one way-specific address tag with an associated valid flag (para. 36), address comparators for comparing an address tag to a memory address, and hit logic driven by outputs of the address comparators and valid flag.

The cache system of Steeley, and that of our application, both take advantage of the subset rule described in Steeley, paragraph 8. Steeley takes advantage of this rule by bypassing higher level cache on a "inval_miss" detection, as described in paragraph 16.

The cache tag system of the present invention differs from that described in Steeley in that Steeley specifically states that "each cache level includes a tag store"; Steeley para. 15, line 8. By this statement, Steeley clearly does not contemplate the present "unified cache tag".

The present "unified cache tag" takes advantage of the subset rule of Steeley in a different way. The present "unified cache tag" does so by using a *unified*, cache tag system, where *each* tag address, and thus tag address comparator, is used to index *two* or more distinct *levels* of cache; this system permits the present system to avoid Steeley's step 732 under some conditions. The key feature lacking in Steeley and

present in all claims (including claims 1-3, 6-8, and 10-11 and claims dependent thereon) of the present application is that Steeley has separate tag system for each cache level, and further that this multiplicity of cache tag systems are not *unified*, in that each tag address and tag address comparator of Steeley is used to index only *one level* of cache.

Claims 1-3 require that each cache tag have associated upper and lower level valid flags. These valid flags indicate presence of valid data in their respective associated cache data memory locations, and drive separate hit logics for each of upper and lower cache levels. Each comparator is coupled to *both* hit logics. This commonality is lacking in Steeley.

In claim 7, the upper and lower level flags and hit logics are associated with separate upper and lower *levels* of cache data memory. As known in the art, these separate levels of cache are typically distinguished by speed and size (Steeley, para. 8). These separate levels of cache may also be distinguished by cache line size, as described in paragraph 43 and claimed in claim 11.

Steeley's inval_miss Flag

An interesting feature in Steeley is an "inval_miss" flag in a lower level cache, that indicates data is *not* valid in higher level cache. Steeley's "inval_miss" flag distinguishes between the possible conditions of "data MAY (but need not) be present in upper level cache," and "data at this point in upper level cache is known not valid". Steeley also has a valid flag in the lower level cache. A cache system having valid and "inval_miss" flags as described in Steeley, requires (when valid=0 and inval_miss=0) access to upper level tag memory to determine whether data is present in upper level cache.

The upper level valid flag of the present application's unified cache differs from the "inval_miss" flag of Steeley in that the upper level valid flag indicates that data is valid in the upper level cache, *without* requiring access to any upper level tag memory to gain additional validity information -- the invention as disclosed has no upper level tag memory. Several claims, including claims 7, 11 and 13, specifically require that the "upper level valid flag" of the unified tag system be capable of indicating that data is valid.

Since it is incapable of indicating data validity by itself, the "inval_miss" flag of Steeley is therefore not an upper level valid flag as defined in the present specification and as the term is used in the claims.

New Claims

Claim 13 is a copy of existing claim 11, with an additional limitation clairifying the meaning of cache level to be that commonly understood in the art; that a lower level of cache is smaller and faster than an upper level cache.

Conclusion

As stated in the remarks above, the art cited by the Examiner fails to anticipate claims 1-3, 6-8, and 10-11. Further, in view of the differences between Steeley and the present invention as claimed, the remaining claims are not obvious in view of Steeley alone or in view of a combination of Steeley and the cited art.

The examiner is therefore respectfully requested to allow the application as amended.

Respectfully submitted,

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